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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,554	WILLIS, DONALD HENRY	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-17,20,21,23-26,29,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-9,11-17,20,21,23,24,26,29,32 and 33* is/are rejected.

7)☒ Claim(s) *3,10 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1,2,4, 6-9,11-17,20,21,23,24, 26, 29, 32, 33** are again rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. U.S. Pat. No. 5,111,297.

Claim **1** is a method claim of claim **14**, and thus, Claim 1 is rejected for the same reasons as in claim 14.

Considering claim **2**, wherein the step of delaying said input video signal includes a step of storing said input video in a delay memory, is met by first frame memory, Fig.6;

Considering claim **4**, wherein said step of alternately supplying said video signal comprises the step of alternately writing said lines of said video signal to said liquid crystal on silicon display.

Regarding claim 4, Tsuji et al. disclose a picture-in-picture double-scanning television receiver. Tsuji et al. do not specifically disclose an LCD display. However, the examiner takes Official Notice in that the LCD display is well known in the art, and,

since Tsuji's output from the second selection circuit is intended to use any well known type of display, it would have been obvious to the skilled in the art to modify the system of Tsuji et al. by providing an LCD display to display the television signals on the LCD monitor, in order to obtain sharper resolution and make the overall system more compact.

Considering claim **6**, wherein the step of storing said video in said delay memory is carried out by storing less than a full frame of video in said delay memory, is met by the second Frame memory 22, fig.6, which stores even or odd fields, i.e., less that a full frame, of the input video signal.

Considering claim **7**, the method of claim 1, comprising the steps of: at least doubling said frame rate of said input video signal; and, writing selected lines of said video signal multiple times to said liquid crystal display, is met by the disclosure that the system "performs a double scanning conversion, thereby providing a sub-picture without causing line flicker." (See Abstract)

Considering claim **8**, the method of claim 1, comprising the step of speeding up said delayed video signal and said input video signal to the same line rate, is met by the disclosure on col. 6, lines 48-52 that "... by reading twice the sub-picture video signal of the same field in reproducing the sub-picture video signal, with the second scanning

being coincident with the first scanning line, a sub-picture without occurrence of line flicker can be attained."

Claim **9**, is a method claim of claim 14, and therefore, Claim 9 is rejected for the same reasons as claim 14.

Considering claim **11**, the method of claim 9, comprising the step simultaneously of 2 writing said lines to top and bottom halves of said display, is met by the disclosure that "a control means which controls (1) read out, from the first and second memory means, either the same field-basis signal twice or the frame-basis signal, and (2) output of the signal read out from the first memory means as the sub-picture video signal for the main scanning line and the signal read out of the second memory means as the sub-picture video signal for the interpolated scanning line". (col.2, line 67 thru col. 3, line 6)

Considering claim **12**, the method of claim 9, comprising the step of 2 propagating said input video signal through a memory embedded 3 in an integrated circuit.

Regarding claim **12**, see rejection of claim 5.

Considering claim **13**, the method of claim 9, comprising the step of 2 speeding up said delayed video signal and said input video signal to the same line rate.

Regarding claim 13, see rejection of claim 7.

Considering claim **14**,

a) a delay memory and a first speed up memory for receiving said input video signal, is met by Second Frame Memory 22 and first frame memory 21, Fig.6; (see also disclosure on col. 6, lines 48-52)

b) a second speed up memory coupled to an output of said delay memory for speeding up said delayed video signal, is met by Line Memory 23, fig.6; (see also col. 6, lines 48-52)

c) a multiplexer coupled to said first and second speed up memories, is met by second selection circuit 26, fig.6;

d) a display coupled to said multiplex, such that portions of video supplied by said multiplexer to said display originate alternately from said first and second speed up memories, is met by the disclosed picture-in-picture double-scanning television receiver which includes the multiplexer circuit 26 which selects alternately from the output of the first frame memory or the output of the first selection circuit through the line memory.

Except for;

e) the claimed display.

Regarding e), see rejection of claim 4.

Considering claim **15**, the frame rate multiplier of claim 14, wherein said delay memory comprises a partial frame memory storing one frame of said video signal;

Regarding claim **15**, Tsuji does not specify how large the memories are. However, it would have been obvious matter of design choice to modify the Tsuji reference by having a first memory that is ½ of a frame or 2/3, ¾ or, 4/5 of a frame, etc. since applicant has not disclosed that having such size difference solve any stated problem or is for any particular purpose and it appears that any other memory would perform equally well.

Considering claim **16**, the frame rate multiplier of claim 14, wherein said speed up memory comprises an array of speed up memories, is met by the Second Frame memory 22, fig.6;

Considering Claim **17**, the frame rate multiplier of claim 14, wherein said delay memory comprises an array of memories, is met by line memory 23, fig.6, which is coupled to Frame Memory 22 and "produces an output signal which is the interpolated scanning line video signal b of the previous line." (col. 6, lines 8-9)

Considering claim **20**, the frame rate multiplier of claim 14, wherein said delay memory and said first speed up memory comprise a single memory;

Regarding claim 20, making separate item integral by functionally combining them is not patentable. (See In re Larson, 144 USPQ 347 (CCPA 1965); see also In Lockhart, 90 USPQ 214 (CCPA 1951))

Considering Claim **21**, the frame rate multiplier of claim **14**, wherein said delay memory and said first and second speed up memories comprise a single memory.

Regarding claim **21**, see rejection of claim 20;

Considering claim **23**, see rejection of claim **14**.

Considering claim **24**, the frame rate doubler of claim **23**, wherein said first memory stores not more than about 1/2 of a frame said video signal.

Regarding claim **24**, see rejection of claim 15;

Considering claim **26**, the frame rate doubler of claim **23**, wherein said liquid crystal display comprises liquid crystal on silicon.

Regarding claim **26**, see rejection of claim 11;

Considering claim **29**, the frame rate doubler of claim 23, wherein said first and second memories are functionally combined into a single memory .

Regarding claim 29, see rejection of claim 20;

Considering claim **32,** the method of claim **1** including a step of storing in said delay memory not more than a portion of said input signal approximately equal to 1/n of a frame of said input video signal, wherein n represents a multiplying factor for said frame rate multiplier, is met by the disclosure "...The circuit consists of a line memory having a storage capacity of 2H (two 1H-capacity line memories in this embodiment), and the operation of one line memory is shown in Chart a and that of another line memory is shown in Chart b. Since both line memories have a read frequency which is twice the write clock frequency, they read out in half the write period 1H. In Chart a, line R is written in 1H period and it is read out twice in the successive two 1/2H periods..." see Col. 7, line 1 through col. 8, lines 43

Considering claim **33,** the frame rate multiplier of claim **14** further comprising a controller coupled to said multiplexer such that said multiplexer is controlled to alternately select a number of successive lines from said first and second speed up memories so as to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display, is met by field polarity discriminator 12, fig.6;

Response to Arguments

3. Applicant's arguments filed July 13, 2004 have been fully considered but they are not persuasive.

Applicant's arguments

a) None of the cited prior art, including Tsuji, discloses a multiplier structure wherein an input video signal is provided to two memories, each memory having different timing functions (a time delay memory and a speed up memory). Tsuji, for example, discloses that second frame 22 an first frame memory 21 of Tsuji Fig.6 serve the same function with respect to the portion of the input signal they contain.

b) Fuji [sic] fails to disclose time delaying the signal in one memory and speeding it up in the other (claim 14), simultaneously providing the input video signal to a delay memory and a speed-up memory (claim 1) and delaying said input video signal for a time less than one frame period (claim 9).

c) Further, Tsuji fails to discloses a display coupled to a multiplexer such that portions of video supplied by the multiplexer to the display originate alternately from first and second speed up memories...

d) Furthermore, Tsuji fails to disclose or suggest a frame memory storing less than one frame of video, nor does Tsuji disclose a frame rate multiplier capable of operating with a frame memory storing less than one frame as claimed in applicant's dependent claims 2 and 15.

Examiner's Response

a) Tsuji et al. disclose a picture-in-picture double-scanning television receiver that stores the video signal in memory (which essentially delays the outputting of the signal from the same memory) and reads the signals from memory twice as fast as the writing speed, essentially speeding up the frame/field rate of the signal. *On col. 6, lines 48-52* Tsuji discloses that "In connection with the arrangement of items (1) and (2), by **reading the same video signal twice continuously from the memory for one-frame period**, while skipping one field of the sub-picture video signal and making the line signal of the main scanning and that of the interpolated scanning to be coincident on the same line, a sub-picture without incurring line flicker can be realized. The provision of a switch for controlling whether field skipping for the sub-picture is performed allows the choice of a sub-picture without line flicker through one-field skipping or a smoother sub-picture using a video signal employing all fields at a risk of line flicker." Therefore, the argument that none of the cited prior art discloses multiplier structure, is unpersuasive.

b) By disclosing the arrangement in Fig.6, Tsuji et al. illustrate that data is read faster than is written. So, the system reads from first frame memory 21 and line memory 23, while the second frame memory 22 is utilized as a delay memory, because inherently storing of a signal in a memory device delays the signal from being output automatically or immediately to the display or other devices further. Note that reading the same video signal twice is equal to speeding up the video signal, i.e. multiplying the frame or field rate of the input video signal.

c) see response in part A.

d) Amended claim **2** recites wherein the step of delaying said input video signal includes a step of storing said input video in a delay memory. Claim 2 **does not** recite "a frame memory storing less than one frame of video" as applicant's representative is arguing in his response. And, furthermore, Claim 5 recites wherein said delay memory comprises *a partial frame memory storing one frame of said video signal*, which is clearly contradictory to say the least. Thus, arguments in this regard do not correspond to the claimed or recited language in claims 2 and 15., and therefore are unpersuasive.

Allowable Subject Matter

4. Claims **3,10, and 25** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a method of multiplying the frame rate of an input video signal comprising: periodically interrupting a supplying step to supply a number of consecutive lines of a speeded up video signal; periodically interrupting said supplying step to supply a number of consecutive lines of a delayed video signal; and, alternating

said interrupting steps to maintain a uniform time interval between writing lines into a same line-number position on a liquid crystal display, as in claims **3** and **10**;

Periodically interrupt a supply of said lines to a liquid crystal display; supply to said liquid crystal display during said periodic interruptions n successive lines from the second memory or n successive lines from a third memory; and, alternately select said n successive lines from said second or third memory in order to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display, as in claim **25**.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
October 3, 2004

MICHAEL H. LEE
PRIMARY EXAMINER